THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte CHING-YUH TSAY,
HUGH P. MCADAMS
and WAHKIT LOH

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Appeal No. 96-4003
Application 08/288,131[1]

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ON BRIEF

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Before BARRETT, FLEMING and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-31 which constitutes all the claims in the application. In response to Appellants' Appeal Brief filed October 11, 1995, the

[1] Application for patent filed August 9, 1994. According to appellants, this application is a continuation of Application 08/083,427, filed June 28, 1993, now abandoned.

Examiner, in the Answer dated January 24, 1996, withdrew the 35 U.S.C. § 112, second paragraph, rejection of claims 22, 24, 26, and 31, indicated the allowability of claims 7-10 and 17-20, and allowed claims 25-31. In addition, the Examiner entered several new grounds of rejection with respect to claims 1-6, 11-16, and 21-24. In a further response to a Reply Brief filed by Appellants on March 11, 1996, the Examiner, in a Supplemental Answer dated May 29, 1996, withdrew the rejection of claims 22 and 24 and indicated their allowability. Accordingly, this appeal now involves only claims 1-6, 11-16, 21, and 23.

The claimed invention relates to a circuit and a method for generating a bias for a semiconductor device. The bias generating circuit includes a plurality of bias circuits responsive to a different enable signal from a control circuit as illustrated in Figure 1 of the drawings. More particularly, Appellants indicate at pages 4 and 5 of the specification that, at any particular time, only one of the bias circuits is enabled by an active enable signal from the control circuit. According to Appellants' specification, the enablement of only one bias circuit for any operational mode results in a reduction of power consumption.

Claim 1 is illustrative of the claimed invention and reads as follows:

1. A circuit for generating a bias for a semiconductor device, the circuit comprising:

a control circuit, responsive to a plurality of input signals, for activating only one of N enable signals at any time, wherein N is greater than one;

a plurality of N bias circuits, each having an output terminal and an enable terminal, the enable

terminal receiving one of the enable signals to enable only one of the bias circuits at any

time for transferring charge between the output terminal and a first reference supply, thereby generating the bias at the output terminal; and

a common bias terminal connected to the output terminal of each of the bias circuits.

The Examiner relies on the following reference:

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| Tobita | 5,065,091 | Nov. 12, 1991 |

Claims 1-6, 11-16, 21, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tobita. Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs and Answers for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection and the evidence of anticipation relied upon by the Examiner as support for the prior art rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answers.

We note that in response to the Examiner's new ground of rejection in the Answer, Appellants separately argue the patentability of independent claims 1 and 11 in the Reply Brief. Since no separate

arguments for patentability have been made with respect to any of the dependent claims 2-6, 12-16, 21, and 23, these claims will stand or fall with their respective base claims.

It is our view, after consideration of the record before us, that the disclosure of Tobita fully meets the invention as set forth in claims 1-6, 11-16, 21, and 23. Accordingly, we affirm. We note that anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claims 1 and 11, the Examiner has indicated how the various limitations are read on the disclosure of Tobita (Answer, pages 4 and 5). In response, Appellants argue several alleged distinctions over Tobita including the contention (Reply Brief, page 3) that, contrary to the present claimed invention, the first and second generated substrate voltages in Tobita are different in magnitude. In support of their position, Appellants refer to the passage at column 12, lines 46-66 of Tobita which describes the different voltages generated by the first and second charge pump circuits.

After careful review of Appellants' arguments, it is our view that such arguments are not

commensurate with the scope of independent claims 1 and 11. It is axiomatic that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation consistent with the specification, and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. In re Sneed, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). Moreover, limitations are not to be read into the claims from the specification. In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The present independent claims 1 and 11 do not require that each bias circuit generate the same bias. Appellants' attempt to attach special significance to the phrases “a bias” and “the bias” as somehow supporting an interpretation of the recited claim language as requiring identical generated bias voltages is not persuasive. As to Appellants’ reference to page 3, lines 7-10 of the their specification as support for their position, we are equally not persuaded that the stated desire for closely regulating the substrate bias voltage would translate into a requirement for the generation of identical output bias voltages from each bias circuit. We agree with the Examiner’s analysis that each of the elements and method steps are shown to exist in the Tobita reference.

Appellants further assert that the circuit of Tobita is directed to a different purpose and for solving a different problem than the instant claimed invention. We note, however, that, to the extent that any statement of intended purpose for Appellants’ circuit appears in the claims, such would not be

persuasive in overcoming the Examiners's established prima facie case of anticipation. A claim containing a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus if the prior art apparatus teaches all the limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In any case, a review of the language of independent claims 1 and 11 reveals that no ultimate intended purpose or use of the bias generating circuit is ever recited. To the contrary, the claimed invention is directed to a circuit and method for generating a bias for a semiconductor device which is precisely the purpose of the circuit of Tobita.

For at least all of the reasons discussed above, the Examiner's 35 U.S.C. § 102(b) rejection of independent claims 1 and 11 is sustained. Further, since the dependent claims stand or fall with their respective base claims, the 35 U.S.C. § 102(b) rejection of dependent claims 2-6, 12-16, 21, and 23 is sustained as well.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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| LEE E. BARRETT | ) | |
| Administrative Patent Judge | ) | |
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| MICHAEL R. FLEMING | ) | INTERFERENCES |
| Administrative Patent Judge | ) | |
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